IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Sang H. Dhong, et al. **Docket:** END920030125US1 (17131)

Serial No.: Unassigned **Dated:** February 12, 2004

Filed: Herewith

For: FAST OPERAND FORMATTING FOR A HIGH PERFORMANCE MULTIPLY-ADD FLOATING POINT-UNIT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

Pursuant to 37 C.F.R. §§1.56, 1.97 and 1.98, applicants submit the following references which applicants believe may be material to the above-identified patent application. A copy of the non-U.S. references which applicants wish to make of record in this case are enclosed herein for the Examiner's convenience along with a listing on Form PTO-1449 attached.

1. U.S. Patent Application Publication No. US 2003/0065698 A1, published April 3, 2003 to Ford;
2. U.S. Patent No. 4,800,516, dated January 24, 1989 to Si, et al.;
3. U.S. Patent No. 5,880,983, dated March 9, 1999 to Elliott, et al.;
4. U.S. Patent No. 5,940,311, dated August 17, 1999 to Dao, et al.;
5. U.S. Patent No. 6,029,243, dated February 22, 2000 to Pontius, et al.;

CERTIFICATE OF MAILING BY "EXPRESS MAIL"

"Express Mail" Mailing Label Number: EU133644686US
Date of Deposit: 4/08/04

I hereby certify that this correspondence is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 C.F.R. §1.10 on the date indicated above and is addressed to the Commissioner of Patents and Trademarks, P.O. Box 1450, Alexandria, VA 22313-1450.

Dated: 4-8-04

Bethany J. Fitzpatrick

A:\17131.ID1.doc

6. U.S. Patent No. 6,044,391, dated March 28, 2000 to Chao, et al.;
7. U.S. Patent No. 6,122,721, dated September 19, 2000 to Goddard, et al.;
8. U.S. Patent No. 6,405,231 B1, dated June 11, 2002 to Nowka, et al.;
9. Lecce, et al., "A VLSI Implementation of a Novel Bit-Serial Butterfly Processor for FFT", *IEEE*, Pages 875-879 - 1991;
10. Luo, et al., "Accelerating Pipelined Integer and Floating-Point Accumulations in Configurable Hardware With Delayed Addition Techniques, *IEEE Transactions On Computers*, Vol. 49, No. 3; Pages 208-218 – March 2000;
11. Yingchun, et al., "A High Speed Microprocessor Core for the Embedded Applications", *IEEE*, Pages 748-751 – 2001;
12. Enriquez, et al., "Design of a Multi-Mode Pipelined Multiplier for Floating-Point Applications", *Air Force Institute of Technology*, Pages 77-81 – February 5, 1991;
13. Inui, et al., "A 250MHz CMOS Floating-Point Divider with Operand Pre-Scaling", *Symposium on VLSI Circuits Digest of Technical Papers*", Pages 17 and 18 – 1999;
14. Lee, et al., "MARS- A RISC-based Architecture for LISP", *IEEE*, Pages 198-206 – 1984; and
15. Namjoo, et al., "CMOS Gate Array Implementation of the Sparc Architecture", *IEEE*, Pages 10-13 – 1988.

All the references listed on Form PTO-1449 are in the English language, thus, a concise explanation of those references required by 37 C.F.R. §1.98(a)(3) is not necessary.

This Information Disclosure Statement is being submitted with the filing of this application; thus no fee or certification under 37 C.F.R. §1.97(e) is required.

Respectfully submitted,

John S Sensny

John S. Sensny
Registration No. 28,757

SCULLY, SCOTT, MURPHY & PRESSER
400 Garden City Plaza
Garden City, New York 11530
(516) 742-4343

JSS:jy

Form PTO-1449 (REV. 7-80) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	Atty. Docket No. END920030125US1 (17131)	Serial No. Unassigned
LIST OF REFERENCES CITED BY APPLICANT (Use several sheets if necessary)	Applicant: Sang H. Dhong, et al.	
	Filing Date: Herewith	Group: Unassigned

U.S. PATENT DOCUMENTS

EXAMINER INITIAL*		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (if appropriate)
	AA	2003/0065698 A1	4/3/03	Ford			
	AB	4,800,516	1/24/89	Si, et al.			
	AC	5,880,983	3/9/99	Elliott, et al.			
	AD	5,940,311	8/17/99	Dao, et al.			
	AE	6,029,243	2/22/00	Pontius, et al.			
	AF	6,044,391	3/28/00	Chao, et al.			
	AG	6,122,721	9/19/00	Goddard, et al.			
	AH	6,405,231 B1	6/11/02	Nowka, et al.			
	AI						

		Foreign Document Number	Date	Country	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO

OTHER PRIOR ART (Including Author, Title, Date, Pertinent Pages, Etc.)

		Lecce, et al., "A VLSI Implementation of a Novel Bit-Serial Butterfly Processor for FFT", *IEEE*, Pages 875-879 - 1991;
		Luo, et al., "Accelerating Pipelined Integer and Floating-Point Accumulations in Configurable Hardware With Delayed Addition Techniques, *IEEE Transactions On Computers*, Vol. 49, No. 3; Pages 208-218 - March 2000;
		Yingchun, et al., "A High Speed Microprocessor Core for the Embedded Applications", *IEEE*, Pages 748-751 - 2001;

EXAMINER	DATE CONSIDERED

*** EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.**

Form PTO-1449 U.S. DEPARTMENT OF COMMERCE
(REV. 7-80)PATENT AND TRADEMARK OFFICE

LIST OF REFERENCES CITED BY APPLICANT

(Use several sheets if necessary)

Atty. Docket No.	Serial No.
END920030125US1 (17131)	Unassigned
Applicant Sang H. Dhong, et al.	
Filing Date Herewith	**Group** Unassigned

U.S. PATENT DOCUMENTS

EXAMINER INITIAL*		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (If appropriate)
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						

		Foreign Document Number	Date	Country	CLASS	SUBCLASS	TRANSLATION	
							YES	NO
							:	

OTHER PRIOR ART (Including Author, Title, Date, Pertinent Pages, Etc.)

		Enriquez, et al., "Design of a Multi-Mode Pipelined Multiplier for Floating-Point Applications", *Air Force Institute of Technology*, Pages 77-81 - February 5, 1991;
		Inui, et al., "A 250MHz CMOS Floating-Point Divider with Operand Pre-Scaling", *Symposium on VLSI Circuits Digest of Technical Papers*", Pages 17 and 18 - 1999;
		Lee, et al., "MARS- A RISC-based Architecture for LISP", *IEEE*, Pages 198-206 - 1984; and

EXAMINER	DATE CONSIDERED

*** EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.**

Form PTO-1449 U.S. DEPARTMENT OF COMMERCE
(REV. 7-80)PATENT AND TRADEMARK OFFICE

LIST OF REFERENCES CITED BY APPLICANT

(Use several sheets if necessary)

Atty. Docket No.	Serial No.
END920030125US1 (17131)	Unassigned
Applicant	
Sang H. Dhong, et al.	
Filing Date	**Group**
Herewith	Unassigned

U.S. PATENT DOCUMENTS

EXAMINER INITIAL*		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (If appropriate)
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						

		Foreign Document Number	Date	Country	CLASS	SUBCLASS	TRANSLATION	
							YES	NO

OTHER PRIOR ART (Including Author, Title, Date, Pertinent Pages, Etc.)

		Namjoo, et al., "CMOS Gate Array Implementation of the Sparc Architecture", *IEEE*, Pages 10-13 - 1988.

EXAMINER	DATE CONSIDERED

*** EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.**